

REMARKS/ARGUMENTS

Claims 1-44 were originally presented.

Claims 1, 6-9, 16, 23, 33, and 42-44 are previously presented.

No claims are currently amended

No claims are canceled.

Claims 1-44 remain in this application.

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39 and 40-44 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,799,168 to Ban (hereinafter "Ban").

Claims 2, 12, 20, 27 and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of U.S. Patent No. 6,000,006 to Bruce *et al.* (hereinafter "Bruce").

Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of U.S. Patent No. 6,493,807 to Martwick (hereinafter "Martwick").

Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39 and 40-44 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of U.S. Patent No. 6,253,281 to Hall *et al.* (hereinafter "Hall").

Claims 2, 12, 20, 27 and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Hall and further in view of Bruce.

Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Hall, further in view of Martwick.

Claims 1-44 remain in this application.

1 **Telephone Conversation with Examiner**

2 Applicant wishes to thank the Examiner for the telephonic conversation on
3 March 7, 2006. In particular Applicant appreciates the Examiner's provisional
4 acceptance of the arguments included below regarding the 35 U.S.C. §102
5 rejections.

6
7 **35 U.S.C. §102(b)**

8 **Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44**

9 Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44 are rejected
10 under 35 U.S.C. §102(b) as being anticipated by Ban. Applicant respectfully
11 traverses the rejection.

12
13 **Independent claim 1 recites:**

14 One or more computer-readable media comprising a flash
15 memory driver that is executable by a computer to interface between
16 a file system and one or more flash memory media, the flash memory
driver comprising:

17 flash abstraction logic that is invokable by the file
system to manage flash memory operations without regard to the
18 type of the one or more flash memory media; and

19 flash media logic configured to interact with different
types of the flash memory media;

20 wherein the flash abstraction logic invokes the flash
media logic to perform memory operations that are potentially
21 performed in different ways depending on the type of the flash
memory media, and further wherein the flash memory driver is flash
22 memory medium agnostic.

23 Ban fails to disclose the one or more computer-readable media comprising a
24 flash memory driver of claim 1. Rather, Ban discloses shifting the responsibility
25 for conforming to the particular requirements of a flash chip from a standardized

1 driver installed on a CPU to a controller *installed on a flash unit*. (Ban, Col. 2,
2 lines 36-38 and 42-46). The standardized driver on the CPU sends out commands
3 necessary to perform flash memory tasks in a uniform, standardized format. (Ban
4 Col. 2, lines 36-38 and 42-43). The standardized commands (read, write, erase and
5 identify) are received via a command register and are translated by the
6 standardized controller *on the flash unit* (through a translating apparatus) into
7 commands specific to the type of flash chip on which the controller is installed.
8 (Ban, Col. 3, lines 1-15 and Col. 5, lines 29-33). Thus, when a flash array
9 including multiple flash chips is used, each flash chip must be provided with a
10 standardized controller customized to interact with only the particular chip *to*
11 *which it is attached*. (Ban, Col. 4, lines 33-35, claim 2 lines 29-30).
12 Consequently, in order for the CPU to communicate with several different types of
13 flash chips, a corresponding number of different, uniquely customized controllers
14 must be utilized on each flash chip.

15 Moreover, the possible output from the CPU is limited to standardized
16 signals. (Ban, Col. 2, lines 41-47). Thus multiple file systems having multiple
17 signal types may not be used under Ban.

18 As a result, Ban fails to disclose “flash abstraction logic that is invokable by
19 the file system to manage flash memory operations without regard to the type of
20 the one or more flash memory media” as recited in claim 1. Rather, under Ban the
21 responsibility for conforming to the requirements of a particular flash chip is given
22 to a uniquely configured standardized controller installed on each particular flash
23 chip. Thus, the controllers disclosed by Ban are flash chip specific, and cannot be
24 used with other types of flash chips. Therefore, each time a new flash chip is used,
25 a new type of standardized controller that is compatible with the new flash chip

1 must be located on the flash chip. Because of this, the controllers disclosed in Ban
2 are ill-equipped “to interact with different types of the flash memory media” as
3 recited in claim 1.

4 Ban also fails to disclose “flash media logic configured to interact with
5 different types of the flash memory media”. As noted above, the controllers
6 disclosed in Ban are flash chip specific. Thus no one controller could interact with
7 several different types of flash chips. Under Ban, such functionality could only be
8 attained by employing a plurality of different controllers – with each flash chip
9 requiring its own distinct type of controller.

10 Moreover, Ban fails to disclose “wherein the flash abstraction logic invokes
11 the flash media logic to perform memory operations that are potentially performed
12 in different ways depending on the type of the flash memory media”. Rather,
13 under Ban the controllers are bound to a particular flash chip and thus are limited
14 to performing memory operations specific to that flash chip only.

15 Additionally, Ban fails to disclose “wherein the flash memory driver is flash
16 memory medium agnostic”. Rather, as noted above, under Ban each standardized
17 controller is bound to a particular flash chip and thus is limited to performing
18 memory operations specific to that flash chip only.

19 In rejecting claim 1, the Office relies on Fig.1, and Col. 2, lines 36-38, Col.
20 4, lines 33-39 as disclosing a flash memory driver (a controller or group of
21 controllers in Ban) comprising flash abstraction logic invokable by a file system to
22 manage flash memory operations without regard to the type of the one or more
23 flash memory media. (*Office Action*, Page 3). Applicant respectfully disagrees.
24 As noted above, controllers, as disclosed in Ban, are flash chip specific, and cannot
25 be used with more than one type of flash chip. Thus any controller disclosed in

1 Ban would only be able to manage flash operations with regard to one specific
2 type of chip, and not “without regard to the type of the one or more flash memory
3 media” as recited in claim 1.

4 The Office also relies on claim 2; the Abstract; Col. 2, lines 36-48; and Col.
5 4, lines 33-39 and 61-65, of Ban as disclosing flash media logic configured to
6 interact with different types of flash memory media (flash chips); wherein the flash
7 abstraction logic invokes the flash media logic to perform memory operations that
8 are potentially performed in different ways depending on the type of the flash
9 memory media. (*Office Action*, Page 3).

10 Again, Applicant respectfully disagrees. Since the controllers taught in Ban
11 are flash chip specific, no one controller could interact with different types of flash
12 memory media or perform memory operations that are potentially performed in
13 different ways depending on the type of flash memory media. Rather, such
14 versatile functionality could only be realized through the utilization of a plurality
15 of different controllers, with each controller corresponding to a different type of
16 flash memory media.

17 Similarly, the Office also relies on Fig. 2 of Ban as disclosing the flash
18 memory driver as being flash memory medium agnostic, and as being located
19 remotely from the flash memory medium (i.e. the flash array in Fig. 1). (*Office*
20 *Action*, Page 3). Again, Applicant respectfully disagrees. Since the controllers
21 taught in Ban are flash chip specific, no one controller could interact with different
22 types of flash memory media or perform memory operations that are potentially
23 performed in different ways depending on the type of flash memory media.
24 Moreover, Ban discloses that each controller is located on the chip it serves.

1 Therefore, each controller can only serve one flash chip and each controller cannot
2 be located remotely from the flash chip it serves.

3 Accordingly, since Ban does not teach all of the elements of claim 1, the
4 §102(b) anticipation rejection of claim 1 based on Ban is not supported. Applicant
5 therefore respectfully requests that the §102(b) rejection of claim 1 be withdrawn.

6 **Dependent claims 5-7** are allowable at the least by virtue of their
7 dependency on base claim 1, as well as for the additional elements they contain.
8 Applicant respectfully requests that the §102(b) rejection of claims 5-7 be
9 withdrawn.

10
11 **Independent claim 9** recites:

12 A flash driver, comprising:
13 flash abstraction logic, interposed between a file
14 system and a flash memory medium, configured to:
15 (a) map a logical sector status from the file system to a
16 physical sector status of the flash memory medium; and
17 (b) maintain memory requirements associated with
18 operating the flash memory medium;
19 wherein the flash driver is located remote from the
20 flash memory medium.

21 Ban fails to disclose the flash driver of claim 9. In particular, as
22 discussed more fully above in conjunction with claim 1, under Ban, each controller
23 is customized for use with a specific flash chip and is necessarily located on the
24 flash chip it serves. This is the opposite of “wherein the flash driver is located
25 remote from the flash memory medium” as recited in claim 9.

In rejecting claim 9, the Office relies on the same bases used in the
rejection of claim 1, namely Fig.1; claim 2; the Abstract; Col. 2, lines 36-48; and

1 Col. 4, lines 33-39 and 61-65 of Ban. (*Office Action*, Page 5). However, the
2 elements of claim 9 are neither disclosed in the cited passages nor anywhere else
3 within Ban. As discussed more fully above, each controller is customized for use
4 with a specific flash chip and is necessarily located on the flash chip it serves.
5 Thus the controllers cannot be located remote from the flash memory medium.

6 Accordingly, since Ban fails to show each and every element of claim 9 the
7 §102(b) rejection of claim 9 based on Ban is not supported. Applicant therefore
8 respectfully requests that the §102(b) rejection of claim 9 be withdrawn.

9 **Dependent claims 10-11** are allowable due to their dependence from an
10 allowable base claim. These claims are also allowable for their own recited
11 features that, in combination with those recited in claim 9, are neither disclosed
12 nor shown in Ban. Applicant therefore respectfully requests that the §102(b)
13 rejection of claims 10 and 11 be withdrawn.

14
15 **Independent claim 16** recites:

16 A flash driver, comprising:
17 user programmable flash medium logic, configured to
18 read, write and erase data to and from a flash memory medium; and
19 flash abstraction logic, interposed between a file
20 system and flash memory medium to maintain universal
21 requirements for the operation of the flash memory medium;
22 wherein the flash memory driver is flash memory
23 medium agnostic.

24 Ban fails to disclose the flash driver of claim 16. Rather, as discussed in
25 more detail above, Ban teaches the use of flash chip specific controllers, such that
for each flash chip used, a separate controller compatible with the flash chip must
be employed on the flash chip. Thus, unlike claim 16, where programmable flash

1 medium logic may be programmed by a user to interact with a flash memory
2 medium, under Ban a new controller must be chosen to interact with each new
3 flash chip.

4 In rejecting claim 16, the Office relies on the same bases used in the
5 rejection of claims 1 and 7 -- namely Fig.1; claim 2; the Abstract; Col. 2, lines 36-
6 48; Col. 4, lines 33-39 and 61-65; and Col. 3, line 49 -- Col. 4, line 13 of Ban.
7 (*Office Action*, Page 5). However, as noted above, Ban fails to disclose or show
8 both "user programmable flash medium logic, configured to read, write and erase
9 data to and from a flash memory medium" and "wherein the flash memory driver
10 is flash memory medium agnostic".

11 Accordingly, Applicant respectfully requests that the §102(b) rejection of
12 claim 16 be withdrawn.

13 **Dependent claims 17 and 22** are allowable at the least by virtue of their
14 dependency on base claim 16, as well as for the additional elements they contain.
15 Applicant respectfully requests that the §102(b) rejection of claims 17 and 22 be
16 withdrawn.

17 **Independent claim 23** recites:

18 A processing device that uses a flash memory medium for
19 storage of data, comprising:

20 a file system, configured to control data storage for the
21 processing device;

22 flash media logic, configured to perform physical sector
23 operations to a flash memory medium based on physical sector
24 commands, wherein the flash medium logic comprises a set of
25 programmable entry points that can be implemented by a user to
interface with any type of flash memory medium selected; and

flash abstraction logic, configured to maintain flash
memory requirements that are necessary to operate the flash memory
medium.

1 Ban fails to disclose the processing device of claim 23. As noted above,
2 under Ban a separate compatible controller must also be used for each flash chip
3 employed. This is different than a flash media logic including "a set of
4 programmable entry points that can be implemented by a user to interface with the
5 type of flash memory medium selected" disclosed in claim 23. One difference lies
6 in the fact that the flash media logic of claim 23 may easily be used with multiple,
7 different flash media. In contrast, under Ban, multiple controllers would be
8 needed to interface with multiple, different flash chips.

9 In rejecting claim 23, the Office relies on Ban, Col. 2, lines 17-23 and 36-
10 48; Col. 3, lines 15-24; and Fig 1. (*Office Action*, Page 4). Applicant respectfully
11 disagrees. As noted above, Ban discloses using different controllers for different
12 flash chips, wherein each controller is located on the flash chip it serves. Thus, a
13 flash medium logic that can interface with several types of flash memory media
14 makes no sense under Ban.

15 In addition, no mention is made in Ban regarding a set of *programmable*
16 *entry points* on the flash medium logic that can be implemented by a user to
17 interface with the type of flash memory medium selected, such as is recited in
18 claim 23.

19 In rejecting this portion of claim 23, the Office relies on Col. 3, lines 15-24.
20 (*Office Action*, Page 4). Applicant respectfully disagrees, as this passage has
21 nothing to do with programmable entry points, and instead discloses a command
22 register on a controller into which a command from the CPU is written before the
23 command is translated by the controller to a command particular to the flash unit to
24 which the controller is attached. Thus, "*programmable entry points* that can be
25

1 implemented by a user to interface with any type of flash memory medium
2 selected” as recited in claim 23 is not disclosed in Ban.

3 Accordingly, Applicant respectfully requests that the §102(b) rejection of
4 claim 23 be withdrawn.

5 **Dependent claims 24-32** are allowable at the least by virtue of their
6 dependency on base claim 23, as well as for the additional elements they contain.
7 Applicant respectfully requests that the §102(b) rejection of claims 24-32 be
8 withdrawn.

9 **Independent claim 33** recites:

10
11 In a processing device that uses a flash memory medium for
12 storage of data, a method for driving the flash memory medium,
comprising:

13 managing rules associated with operating the flash
memory medium in a flash abstraction logic; and

14 issuing physical sector commands directly to the flash
memory medium from a flash medium logic;

15 wherein the method is flash memory medium agnostic.
16

17 Ban fails to disclose the processing device of claim 33. In particular, as
18 noted above, under Ban a separate, unique controller must be used for each flash
19 chip employed. This is different than “wherein the method is flash memory
20 medium agnostic” disclosed in claim 33. The difference lies in the fact that the
21 flash media logic of claim 33 may easily be used with multiple, different flash
22 media. In contrast, under Ban, multiple controllers would be needed to interface
23 with multiple, different flash chips.

24 The Office argues that the claimed method for driving the flash memory
25 medium is shown in Fig.1; claim 2; the Abstract; Col. 2, lines 36-48; claim 7; Col.

1 3, lines 19-24 of Ban; Col. 4, lines 33-29 and 61-65; and Col. 3, line 49-Col. 4,
2 line 13 of Ban. (*Office Action*, Page 6). Applicant respectfully disagrees. As
3 noted above, under Ban a unique controller must be used for each flash chip, with
4 each controller being located on the flash chip it serves. Thus, a flash memory
5 medium agnostic method as recited in claim 33 makes no sense under Ban.
6 Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 33
7 be withdrawn.

8 **Dependent claims 37 and 39-41** are allowable at the least by virtue of their
9 dependency on base claim 33, as well as for the additional elements they contain.
10 Applicant respectfully requests that the §102(b) rejection of claims 37 and 39-41
11 be withdrawn.

12 **Independent claim 42** recites:

13
14 A computer-readable medium for a flash driver, comprising
15 computer-executable instructions that, when executed, direct the
16 flash driver to provide an interface between a file system, selected
17 from one of a plurality of different file systems, and a flash memory
18 medium, selected from one of a plurality of different flash memory
media, wherein the flash driver is located remote from the flash
memory medium.

19 Ban fails to disclose the computer readable medium for a flash driver of
20 claim 42. As discussed above, under Ban a separate, unique controller must be
21 used for each flash chip employed, with each controller being located on the flash
22 chip it serves. This is different than “the flash driver to provide an interface
23 between a file system, selected from one of a plurality of different file systems, and
24 a flash memory medium, selected from one of a plurality of different flash memory
25

1 media” and “the flash driver is located remote from the flash memory medium”
2 disclosed in claim 42.

3 In rejecting claim 42, the Office relies on the same bases used to reject
4 claim 1 -- Fig. 1; claim 2; the Abstract; and Col. 2, lines 36-48 of Ban. (*Office*
5 *Action*, Page 5). Applicant respectfully disagrees. As discussed in more detail
6 above, these passages disclose placing separate controllers on each flash chip in a
7 flash array in order to interface with a CPU. Thus no one controller can interface
8 with “a flash memory medium, selected from one of a plurality of different flash
9 memory media” as recited in claim 42. Instead, under Ban, a plurality of
10 controllers would be required to fulfill such a function. Moreover, none of the
11 controllers disclosed in Ban are located remote from the flash memory medium.
12 Accordingly, Applicant respectfully requests that the §102(b) rejection of claim 42
13 be withdrawn.

14
15 **Independent claim 43** recites:

16 A computer-readable medium for a flash driver, comprising
17 computer-executable instructions that, when executed, direct the
18 flash driver to:

19 provide an interface between a file system, selected
20 from one of a plurality of different files systems, and a flash memory
21 medium, selected from one of a plurality of different flash memory
22 media; and

23 manage a set of characteristics that are common to the
24 plurality of different flash memory media at a flash abstraction logic;
25 wherein the flash driver is flash memory medium
agnostic.

26 Ban fails to disclose the computer-readable medium for a flash driver of
27 claim 43. Similar to claim 42 above, under Ban, the responsibility for conforming

1 to the particular requirements of each flash chip is given to a controller installed on
2 each flash chip. Thus the controllers used under Ban are flash chip specific, and
3 can provide an interface for only one chip. Therefore, a single controller under
4 Ban cannot provide an interface between “one of a plurality of different flash
5 memory media” as disclosed in claim 43. Rather, under Ban, in order to provide
6 an interface with more than one different flash chip, an equivalent number of
7 controllers would be needed, with a unique controller being located on each flash
8 chip. Therefore Ban does not disclose “provide an interface between a file system,
9 selected from one of a plurality of different files systems, and a flash memory
10 medium, selected from one of a plurality of different flash memory media” as
11 recited in claim 43.

12 Moreover, since the controllers disclosed in Ban are flash chip specific, it
13 would take a plurality of controllers to manage characteristics common to a
14 plurality of flash chips. Therefore, Ban does not disclose a flash driver which can
15 “manage a set of characteristics that are common to the plurality of different flash
16 memory media at a flash abstraction logic” as is recited in claim 43. Rather, under
17 Ban a plurality of controllers having flash abstraction logic would be required to
18 fulfill this function.

19 Additionally, since each controller is located on a corresponding flash chip,
20 and exclusively serves only that flash chip, “wherein the flash driver is flash
21 memory medium agnostic” makes no sense under Ban.

22 The Office argues that the same passages cited with regard to claim 42
23 above disclose the claimed computer-readable medium claimed in claim 43.
24 (*Office Action*, Page 5). Applicant respectfully disagrees. As noted above, these
25 passages disclose placing separate controllers on each flash chip in an array in

1 order to interface with a CPU. Thus, under Ban no one controller can interface
2 with a flash memory medium, selected from one of a plurality of different flash
3 memory media, and no one controller can manage a set of characteristics common
4 to a plurality of different flash memory media at a flash abstraction logic. Nor is
5 any one controller flash memory medium agnostic.

6 Accordingly, Applicant respectfully requests that the §102(b) rejection of
7 claim 43 be withdrawn.

8
9 **Independent claim 44** recites:

10 A computer-readable medium for a flash driver, comprising
11 computer-executable instructions that, when executed, direct the
flash driver to:

12 provide an interface between a file system, selected
13 from one of a plurality of different files systems, and a flash memory
medium, selected from one of a plurality of different flash memory
14 media;

15 manage a set of characteristics that are common to the
plurality of different flash memory media at a flash abstraction logic;
and

16 provide programmable entry points that can be
17 optionally selected by a user to interface with the type of flash
memory medium selected;

18 wherein the flash driver is located remote from the
flash memory medium and the flash driver is flash memory medium
19 agnostic.

20
21 Ban fails to disclose the computer-readable medium for a flash driver of
22 claim 44. As discussed above, under Ban a single controller cannot provide an
23 interface between “a file system, selected from one of a plurality of different files
24 systems, and a flash memory medium, selected from one of a plurality of different
25 flash memory media”. Moreover, it also follows that a controller under Ban

1 cannot "manage a set of characteristics that are common to the plurality of
2 different flash memory media at a flash abstraction logic". To achieve this sort of
3 functionality, Ban would require a plurality of controllers rather than the single
4 flash driver recited in claim 44.

5 In addition, since a controller under Ban is configured to interface with a
6 particular flash chip -- and is even located on a particular flash chip -- a controller
7 under Ban could not be used to "provide programmable entry points that can be
8 optionally selected by a user to interface with the type of flash memory medium
9 selected". This would imply that a controller disclosed in Ban could work with
10 several different flash chips, which it can't. Moreover, there is no disclosure in
11 Ban which mentions "programmable entry points that can be optionally selected by
12 a user". Rather, under Ban the user is limited to the use of a specific controller
13 adapted to operate with a specific flash chip. No other choice is possible.

14 Additionally, since each controller is uniquely configured for the flash chip
15 on which it is located, a "flash driver is located remote from the flash memory
16 medium and the flash driver is flash memory medium agnostic" makes no sense
17 under Ban.

18 The Office rejects claim 43 on the same bases used in rejecting claim 1 --
19 Fig.1, and Col. 2, lines 33-39 and 61-65, Col. 4, lines 33-39, claim 2, and the
20 Abstract (*Office Action*, Pages 2, 3 and 5). Applicant respectfully disagrees. Ban
21 discloses only controllers that are configured for one specific type of flash chip.
22 Thus the versatility recited in claim 44 above would be impossible under Ban.
23 Moreover, nowhere does Ban disclose "programmable entry points that can be
24 optionally selected by a user to interface with the type of flash memory medium
25 selected". Furthermore, since each controller under Ban is uniquely configured for

1 the flash chip on which it is located, a “flash driver is located remote from the
2 flash memory medium and the flash driver is flash memory medium agnostic”
3 makes no sense under Ban. Accordingly, Applicant respectfully requests that the
4 §102(b) rejection of claim 44 be withdrawn.

5
6 **35 U.S.C. §103(a)**

7 The remaining claims are rejected under a set of §103 rejections, all of which
8 rely on Ban as the primary reference. Moreover, all of these claims depend from
9 base claims addressed above.

10
11 **Ban +Bruce**

12 Claims 2, 12, 20, 27 and 35 are rejected under 35 U.S.C. §103(a) as being
13 unpatentable over Ban in view of Bruce. Applicant respectfully traverses the
14 rejection.

15 Claims 2, 12, 20, 27 and 35 depend from respective independent claims 1,
16 9, 16, 23, and 33. As such, they include the features recited in those base claims.
17 The combination of Ban and Bruce fails to teach or suggest the features of these
18 base claims from which the cited claims depend. Ban is primarily cited as teaching
19 the base features, and Bruce is cited as teaching the use of a unified remapping and
20 wear leveling table to overcome the disadvantages of the larger granularity of
21 block remapping.

22 With respect to **dependent claim 2**, neither reference discloses, “flash
23 media logic configured to interact with different types of the flash memory media”
24 or “wherein the flash abstraction logic invokes the flash media logic to perform
25 memory operations that are potentially performed in different ways depending on

1 the type of the flash memory media". Instead, as discussed above, Ban teaches
2 that the controllers are bound to a particular flash chip and thus are limited to
3 performing memory operations specific to that flash chip. Thus interacting with
4 different types of flash memory media would require several controllers rather than
5 the single flash memory driver recited in claim 1 from which claim 2 depends.

6 Bruce offers no missing teaching. Accordingly, the combination of Ban
7 and Bruce fails to teach or suggest the device of claim 2. Applicant respectfully
8 requests that the §103 rejection of claim 2 be withdrawn.

9 With respect to **dependant claim 12**, neither reference discloses "flash
10 abstraction logic, interposed between a file system and a flash memory medium,
11 configured to: (a) map a logical sector status from the file system to a physical
12 sector status of the flash memory medium" as recited by claim 9 from which claim
13 12 depends. Rather Ban teaches the opposite of this by disclosing that during a
14 read write operation the CPU specifies the flash address at which a read/write
15 operation shall take place. Thus, under Ban the CPU, rather than the flash driver,
16 coordinates and organizes all mappings between a computer's file system (using,
17 for example, logical sector addressing) and the flash array (using, for example,
18 physical sector addressing).

19 Again, Bruce offers no missing teaching. Accordingly, the combination of
20 Ban and Bruce fails to teach or suggest the device of claim 12. Applicant
21 respectfully requests that the §103 rejection of claim 12 be withdrawn.

22 With respect to **dependant claim 20**, for the reasons just given, neither Ban
23 nor Bruce teaches or suggests "user programmable flash medium logic, configured
24 to read, write and erase data to and from a flash memory medium". Accordingly,
25

1 the combination of Ban and Bruce fails to teach or suggest the device of claim 20.
2 Applicant respectfully requests that the §103 rejection of claim 20 be withdrawn.

3 With respect to **dependant claim 27**, neither Ban nor Bruce teaches or
4 suggests “a set of programmable entry points that can be implemented by a user to
5 interface with the type of flash memory medium selected” as recited in claim 23
6 from which claim 27 depends. Ban teaches that a separate compatible controller
7 must be used for each flash chip employed, with each controller being attached to
8 the flash chip it serves. This teaches away from the processing device of claim 27
9 which may be used with multiple, different flash chips. In contrast, under Ban,
10 multiple controllers would be needed to interface with multiple flash chips.

11 Again, Bruce offers no relevant teaching. Applicant respectfully requests
12 that the §103 rejection of claim 27 be withdrawn.

13 With respect to **dependant claim 35**, neither reference discloses, teaches or
14 suggests “issuing physical sector commands directly to the flash memory medium
15 from a flash medium logic” as recited in claim 33 from which claim 35 depends.
16 Ban teaches that during a read write operation the CPU specifies the flash address
17 at which a read/write operation shall take place. Thus, Ban teaches away from
18 claim 33 and claim 35, which depends from claim 33, by specifying that the CPU,
19 rather than the flash driver, must coordinate and organize all mappings between a
20 computer’s file system (using, for example, logical sector addressing) and the flash
21 array (using, for example, physical sector addressing).

22 Again, Bruce offers no relevant teaching. Applicant respectfully requests
23 that the §103 rejection of claim 35 be withdrawn.

1
2 **Ban + Martwick**

3 Claims 3-4, 13-14, 19, 21, 26, 28, 34, and 36 are rejected under 35 U.S.C.
4 §103(a) as being unpatentable over Ban in view of Martwick. Applicant
5 respectfully traverses the rejection.

6 Claims 3-4, 13-14, 19, 21, 26, 28, 34, and 36 depend from respective
7 independent claims 1, 9, 16, 23, and 33. As such, they include the features recited
8 in those base claims. The combination of Ban and Martwick fails to teach or
9 suggest the features of the base claims from which the cited claims depend. Ban is
10 primarily cited as teaching the base features, and Martwick is cited as teaching a
11 method for updating flash blocks so that data integrity gets maintained and data
12 can be recovered upon a power failure.

13 **Dependent claims 3 and 4** depend from claim 1, and hence include the
14 features therein. Neither Ban nor Martwick disclose, “flash abstraction logic that
15 is invokable by the file system to manage flash memory operations without regard
16 to the type of the one or more flash memory media” as recited in claim 1. As noted
17 above, Ban specifically teaches giving the responsibility for conforming to the
18 particular requirements of a flash chip to a controller installed on an individual
19 flash chip. Thus the controllers used under Ban are flash chip specific, and cannot
20 be used with other types of flash chips. Therefore, each time a new flash chip is
21 used, a new controller that is compatible with the new flash chip must be located
22 on the flash chip.

23 In addition, neither reference discloses, teaches or suggests “flash media
24 logic configured to interact with different types of the flash memory media” or
25 “wherein the flash abstraction logic invokes the flash media logic to perform

1 memory operations that are potentially performed in different ways depending on
2 the type of the flash memory media". Instead, Ban teaches that the controllers are
3 bound to a particular flash chip and thus are limited to performing memory
4 operations specific to that flash chip. Thus interacting with different types of flash
5 memory media would require several controllers rather than the single flash
6 memory driver recited in claim 1 from which claims 3 and 4 depend.

7 Martwick fails to add any relevant teaching with respect to these features.
8 Accordingly, the combination of Ban and Martwick fails to teach or suggest the
9 device of claims 3 and 4. Applicant respectfully requests that the §103 rejection of
10 claims 3 and 4 be withdrawn.

11 Similarly **dependant claims 13 and 14** depend from base claim 9 and thus
12 include the features therein. Ban fails to teach or suggest "flash abstraction logic,
13 interposed between a file system and a flash memory medium, configured to: (a)
14 map a logical sector status from the file system to a physical sector status of the
15 flash memory medium" as recited in claim 9 from which claims 13 and 14 depend.
16 As previously discussed, Ban teaches away from this by disclosing that during a
17 read/write operation the CPU specifies the flash address at which a read/write
18 operation shall take place. Thus, under Ban the CPU, rather than the flash driver,
19 coordinates and organizes all mappings between a computer's file system (using,
20 for example, logical sector addressing) and the flash array (using, for example,
21 physical sector addressing).

22 Again, Martwick offers no missing teaching. Accordingly, the combination
23 of Ban and Martwick fails to teach or suggest the device of claims 13 and 14.
24 Applicant respectfully requests that the §103 rejection of claims 13 and 14 be
25 withdrawn.

1 **Dependant claims 19 and 21** depend from base claim 16 and hence include
2 the features therein. For the reasons just given, neither reference teaches or
3 suggests “user programmable flash medium logic, configured to read, write and
4 erase data to and from a flash memory medium”. Accordingly, the combination of
5 Ban and Martwick fails to teach or suggest the devices of claims 19 and 21.
6 Applicant respectfully requests that the §103 rejection of claims 19 and 21 be
7 withdrawn.

8 **Dependant claims 26 and 28** depend from base claim 23 and hence include
9 the features therein. Neither reference teaches or suggests “a set of programmable
10 entry points that can be implemented by a user to interface with any type of flash
11 memory medium selected” as recited in claim 23 from which claims 26 and 28
12 depend. Instead, Ban teaches that a separate compatible controller must be used
13 for each flash chip employed. This teaches away from the processing device of
14 claims 26 and 28, which may be used with multiple, different flash chips. In
15 contrast, under Ban multiple controllers would be needed to interface with multiple
16 flash chips. Moreover, Ban fails to teach a set of programmable entry points as
17 recited in claim 23.

18 Again, Martwick offers no relevant teaching. Applicant respectfully
19 requests that the §103 rejection of claims 26 and 28 be withdrawn.

20 Similarly, **dependant claims 34 and 36** depend from base claim 33 and
21 hence include the features therein. Neither reference discloses, teaches or suggests
22 “issuing physical sector commands directly to the flash memory medium from a
23 flash medium logic” as recited in claim 33 from which claims 33 and 36 depend.
24 Instead, Ban teaches that during a read write operation the CPU specifies the flash
25 address at which a read/write operation shall take place. Thus, Ban teaches away

1 from claims 33, 34 and 36 by specifying that the CPU, rather than the flash driver,
2 must coordinate and organize all mappings between a computer's file system
3 (using, for example, logical sector addressing) and the flash array (using, for
4 example, physical sector addressing).

5 Again, Martwick offers no relevant teaching. Applicant respectfully
6 requests that the §103 rejection of claims 34 and 36 be withdrawn.

7
8 **Ban + Hall**

9 Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44 are rejected
10 under 35 U.S.C. §103(a) as being unpatentable over Ban in view of Hall.
11 Applicant respectfully traverses the rejection.

12 Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44 depend from
13 respective independent claims 1, 9, 16, 23, and 33. As such, they include the
14 features recited in those base claims. The combination of Ban and Hall fails to
15 teach or suggest the features of the base claims from which the cited claims
16 depend. Ban is primarily cited as teaching the base features, and Hall is cited as
17 teaching a flash memory medium agnostic flash driver, a flash driver located
18 remote from the flash memory medium, and flash media logic that is configured to
19 interact with different types of flash memory media.

20 As noted above, Ban fails to teach several elements in claims 1, 9, 16, 23,
21 and 33, including a flash memory driver which is memory medium agnostic, a
22 flash driver located remote from the flash memory medium, and a flash medium
23 logic comprising a set of programmable entry points that can be implemented by a
24 user to interface with any type of flash memory medium selected. Moreover, as
25 also discussed above, Ban teaches shifting the responsibility for conforming to the

1 particular requirements of a flash chip from a standardized driver installed on a
2 CPU to a controller *installed on a flash unit*. According to Ban, the standardized
3 driver on the CPU sends out generic commands (read, write, erase and identify) in
4 a uniform, standardized format which are received via a command register and are
5 translated by the standardized controller *on the flash unit* (through a translating
6 apparatus) into commands specific to the type of flash chip on which the controller
7 is installed. Thus, when a flash array including multiple flash chips is used, each
8 flash chip must be provided with a standardized controller customized to interact
9 with only the particular chip *to which it is attached*. Consequently, in order for the
10 CPU to communicate with several different types of flash chips, a corresponding
11 number of different, uniquely customized controllers must be utilized on each flash
12 chip.

13 In contrast, Hall teaches sending command-type signals from a processor
14 directly to a flash memory, with the signals being tailored by the processor to be
15 compatible with the specific type of flash memory. (Col. 1, line 61- Col 2, line 16;
16 and Col. 3, lines 51-59). This is the exact opposite of the behavior of the CPU
17 taught in Ban, which sends standardized signals *to be later* translated by
18 controllers located on flash chips. Thus, there is no motivation to combine Ban
19 with Hall, and in fact, Ban teaches away from combination with Hall by
20 contradicting the teachings of Hall. Accordingly, Hall may not be properly
21 combined with Ban. On this basis alone, Applicant respectfully requests that the
22 §103 rejection of claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39, and 40-44 be
23 withdrawn.

24 Moreover, both Ban and Hall, either alone or in combination, fail to
25 disclose, teach or suggest a flash medium logic comprising a set of programmable

1 entry points that can be implemented by a user to interface with any type of flash
2 memory medium selected. Thus, even if Ban and Hall could be combined, they
3 would fail to teach or suggest all of the elements found in claim 22, claim 23 (from
4 which claims 24-32 depend), and claims 30, 38, 39 and 44. On this basis alone,
5 Applicant respectfully requests that the §103 rejection of claims 22-25, 29, 31-32,
6 39, and 44 be withdrawn.

8 **Ban + Hall + Bruce**

9 Claims 2, 12, 20, 27 and 35 are rejected under 35 U.S.C. §103(a) as being
10 unpatentable over Ban in view of Hall, and further in view of Bruce. Applicant
11 respectfully traverses the rejection.

12 Claims 2, 12, 20, 27 and 35 depend from respective independent claims 1,
13 9, 16, 23, and 33. As such, they include the features recited in those base claims.
14 As noted above, there is no motivation to combine Ban with Hall, and in fact, Ban
15 teaches away from combination with Hall by contradicting the teachings of Hall.
16 Accordingly, Hall may not be properly combined with Ban. And, as also discussed
17 above, Ban fails to disclose, teach or suggest the elements of claims 1, 9, 16, 23,
18 and 33, and Bruce fails to add any of Ban's missing teachings. On this basis alone,
19 Applicant respectfully requests that the §103 rejection of claims 2, 12, 20, 27 and
20 35 be withdrawn.

21 Moreover, Ban, Hall, and Bruce, either alone or in combination, fail to
22 disclose, teach or suggest a flash medium logic comprising a set of programmable
23 entry points that can be implemented by a user to interface with any type of flash
24 memory medium selected. Thus, even if Ban and Hall could be combined, they, in
25 combination with Bruce, would fail to teach or suggest all of the elements found in

1 claims 27. On this basis alone, Applicant respectfully requests that the §103
2 rejection of claim 27 be withdrawn.

3
4 **Ban + Hall + Martwick**

5 Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C.
6 §103(a) as being unpatentable over Ban in view of Hall, and further in view of
7 Martwick. Applicant respectfully traverses the rejection.

8 Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 depend from respective
9 independent claims 1, 9, 16, 23, and 33. As such, they include the features recited
10 in those base claims. As noted above, there is no motivation to combine Ban with
11 Hall, and in fact, Ban teaches away from combination with Hall by contradicting
12 the teachings of Hall. Accordingly, Hall may not be properly combined with Ban.
13 Moreover, as also discussed above, Ban fails to disclose, teach or suggest the
14 elements of claims 1, 9, 16, 23, and 33, and Martwick fails to add any of Ban's
15 missing teachings. On this basis alone, Applicant respectfully requests that the
16 §103 rejection of claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 be withdrawn.

17 Moreover, Ban, Hall, and Martwick, either alone or in combination, fail to
18 disclose, teach or suggest a flash medium logic comprising a set of programmable
19 entry points that can be implemented by a user to interface with any type of flash
20 memory medium selected. Thus, even if Ban and Hall could be combined, they, in
21 combination with Martwick, would fail to teach or suggest all of the elements
22 found in claims 26 and 28. On this basis alone, Applicant respectfully requests
23 that the §103 rejection of claims 26 and 28 be withdrawn.

1 **CONCLUSION**

2 All pending claims 1-44 are in condition for allowance. Applicant
3 respectfully requests reconsideration and prompt issuance of the subject
4 application. If any issues remain that prevent issuance of this application, the
5 Examiner is urged to contact the undersigned attorney before issuing a subsequent
6 Action.

7
8 Respectfully Submitted,

9
10 Dated: April 21, 2006

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